Bahria University,

Karachi Campus



LAB EXPERIMENT NO.

**\_\_\_\_\_\_\_\_10\_\_\_\_\_\_**

LIST OF TASKS

|  |  |
| --- | --- |
| TASK NO | OBJECTIVE |
| 01 | Verify the operation of NOT, AND, OR, NAND and NOR Gates using MultiSim and attach the circuit snapshots? |
| 02 | Implement the following equations on MultiSim and verify through Truth Table:   1. **(**ACD) + (A ( B + C)) + (BC) + (ABD) + (B) 2. (A+ + C). ( + + D).(B+ C + ) |
|  |  |

Submitted On:

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(Date: DD/MM/YY)

Task # 01: Verify the operation of NOT, AND, OR, NAND and NOR Gates using MultiSim and attach the circuit snapshots?

Solution:

NOT:

A picture containing text, light, decorated, colors

Description automatically generated

Background pattern

Description automatically generated

AND:

A picture containing diagram

Description automatically generated

A picture containing timeline

Description automatically generated

OR:

Diagram, timeline

Description automatically generated

Diagram

Description automatically generated

NAND:

Diagram

Description automatically generated

Diagram

Description automatically generated

NOR:

A picture containing diagram

Description automatically generated

Diagram

Description automatically generated with low confidence

Task # 02: Implement the following equations on MultiSim and verify through Truth Table:

**a) (**ACD) + (A ( B + C)) + (BC) + (ABD) + (B)

Solution:

Circuit Diagram :

Diagram, schematic

Description automatically generated

Truth Table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **(ACD) + (A ( B + C)) + (BC) + (ABD) + (B)** |
| 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 0 |
| 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 |

b) (A+ + C). ( + + D).(B+ C + )

Solution :

Circuit Diagram :

Diagram, schematic

Description automatically generated

Truth Table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **(A+ + C). ( + + D).(B+ C + )** |
| 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |